

**What is claimed is:**

1           1. An integrated circuit, comprising:  
2                 one or more memory cells, each memory cell  
3     comprising first and second p-channel transistor and first  
4     and second n-channel transistors configured as cross-coupled  
5     logic inverters between first and second reference voltage  
6     levels during a normal mode of operation; and  
7                 power control circuitry coupled to a source  
8     terminal of the first p-channel transistor of each memory  
9     cell, for providing to the first p-channel transistors the  
10    first reference voltage level during the normal mode of  
11    operation, and causing a first voltage less than the first  
12    reference voltage level to appear at the source terminal of  
13    the first p-channel transistors during a data corruption mode  
14    of operation wherein data stored in the one or more memory  
15    cells is corrupted.

1           2. The integrated circuit of claim 1, wherein the power  
2     control circuitry is coupled to a source terminal of the  
3     second p-channel transistor of each memory cell, for  
4     providing to the first p-channel transistor the first  
5     reference voltage level during the normal mode of operation,  
6     and the first voltage during the data corruption mode of  
7     operation.

1           3. The integrated circuit of claim 1, wherein the power  
2     control circuitry is coupled to a source terminal of at least  
3     one of the first and second n-channel transistor, for  
4     providing to the at least one of the first and second n-  
5     channel transistors the second reference voltage level during  
6     the normal mode of operation, and for causing a second  
7     voltage greater than the second reference voltage level to  
8     appear on the source terminal of at least one of the first  
9     and second n-channel transistors during the data corruption  
10    mode of operation.

1           4. The integrated circuit of claim 3, wherein the at  
2     least one of the first and second n-channel transistor has  
3     a drain terminal coupled to a drain terminal of the second  
4     p-channel transistor.

1           5. The integrated circuit of claim 3, wherein, during  
2 the data corruption mode of operation, the power control  
3 circuitry pulses the source terminal of the first p-channel  
4 transistor of each memory cell to the first voltage, and  
5 pulses the source terminal of the at least one of the first  
6 and second n-channel transistors to the second voltage, the  
7 pulses partially overlapping.

1           6. The integrated circuit of claim 5, wherein, during  
2 the data corruption mode of operation, a leading edge of the  
3 pulse corresponding to the first p-channel transistor occurs  
4 prior to a leading edge of the pulse corresponding to the at  
5 least one of the first and second n-channel transistors.

1           7. The integrated circuit of claim 6, wherein, during  
2 the data corruption mode of operation, a trailing edge of the  
3 corresponding to the first p-channel transistor occurs prior  
4 to a trailing edge of the pulse corresponding to the at least  
5 one of the first and second n-channel transistors.

1           8. The integrated circuit of claim 5, wherein the power  
2     control circuitry temporarily shorts the source terminal of  
3     the first p-channel transistor in each memory cell to the  
4     source terminal of the at least one of the first and second  
5     n-channel transistors in each memory cell.

1           9. The integrated circuit of claim 8, wherein the power  
2     control circuitry comprises at least one first control  
3     transistor coupled between the source terminal of the first  
4     p-channel transistor of each memory cell to the source  
5     terminal of the at least one of the first and second n-  
6     channel transistors of each memory cell.

1           10. The integrated circuit of claim 8, wherein the  
2     power control circuitry further comprises at least one second  
3     control transistor coupled between the first reference  
4     voltage level and the source terminal of the first transistor  
5     of each memory cell, and at least one third control  
6     transistor coupled between the second reference voltage level  
7     and the source terminal of the at least one of the first and  
8     second n-channel transistors of each memory cell.

1           11. The integrated circuit of claim 1, wherein the  
2 first voltage is the second reference voltage level.

1           12. The integrated circuit of claim 1, wherein the  
2 first voltage is a voltage resulting from the source terminal  
3 of the first p-channel transistor of each memory cell being  
4 in an undriven state during the data corruption mode of  
5 operation.

1           13. The integrated circuit of claim 1, wherein each  
2 memory cell further comprises at least one pass gate  
3 transistor having a conduction terminal coupled to at least  
4 one bit line and a control terminal coupled to a word line,  
5 and the power control circuitry drives the bit lines to a  
6 voltage corresponding to a predetermined logic value and  
7 drives each word line to a voltage to activate each pass gate  
8 transistor during the data corruption mode of operation when  
9 the source terminal of the first p-channel transistor of each  
10 memory cell is at the first voltage.

1           14. A method of corrupting data values stored in a  
2           plurality of memory cells coupled between at least one first  
3           node and at least one second node, the method comprising:  
4                    decoupling the at least one first node from a first  
5           reference voltage level and causing a first voltage less than  
6           the first reference voltage level to appear on the at least  
7           one first node; and  
8                    following the step of decoupling, driving the at  
9           least one first node towards the first reference voltage  
10          level.

1           15. The method of claim 14, further comprising driving  
2           the at least one second node to a second reference voltage  
3           level during the step of driving the at least one first node.

1           16. The method of claim 15, further comprising  
2           decoupling, during at least a portion of the time the at  
3           least one first node is decoupled from the first reference  
4           voltage level and prior to the step of driving the at least  
5           one second node, the at least one second node from the second  
6           reference voltage level and causing a second voltage greater  
7           than the second reference voltage level to appear on the at  
8           least one second node.

1           17. The method of claim 16, wherein the step of causing  
2   a second voltage comprises driving the at least one second  
3   node to the second voltage.

1           18. The method of claim 16, wherein the second voltage  
2   is the first reference voltage level.

1           19. The method of claim 16, wherein the step of  
2   decoupling the at least one second node occurs after the step  
3   of decoupling the at least one first node.

1           20. The method of claim 16, further comprising shorting  
2   the at least one first power supply node to the at least one  
3   second power supply node following the steps of decoupling  
4   the at least one first power supply node and the at least one  
5   second power supply node.

1           21. The method of claim 15, wherein the first voltage  
2   is the second reference voltage level.

1           22. The method of claim 14, wherein the step of causing  
2   a first voltage comprises driving the at least one first  
3   power supply node to the first voltage.

1           23. A system, comprising:  
2                a processing unit; and  
3                one or more memory cells coupled to the processing  
4   unit, each memory cell capable of storing one or more data  
5   values therein and being coupled to first and second power  
6   supply nodes; and  
7                power control circuitry, coupled to the one or more  
8   memory cells, for placing a first reference voltage on the  
9   first power supply node and a second reference voltage on the  
10   second power supply node during a normal mode of operation,  
11   and causing a first voltage less than the first reference  
12   voltage to appear on the first power supply node during a  
13   data corruption mode of operation wherein the one or more  
14   data values stored in each of the one or more memory cells  
15   are corrupted.

1           24. The system of claim 23, wherein the first voltage  
2   is the second reference voltage.



1           25. The system of claim 23, wherein each memory cell  
2 comprises first and second p-channel transistors and first  
3 and second n-channel transistors configured as a logic  
4 inverter during the normal mode of operation, the first p-  
5 channel transistor having a source terminal coupled to the  
6 first power supply node.

1           26. The system of claim 25, wherein a source terminal  
2 of the second p-channel transistor of each memory cell is  
3 coupled to a third power supply node, the third power supply  
4 node having the first reference voltage during the normal and  
5 data corruption modes of operation.

1           27. The system of claim 26, wherein the power control  
2 circuitry comprises a logic inverter having an output coupled  
3 to the first power supply node.

1           28. The system of claim 26, wherein the power control  
2 circuitry comprises a transistor coupled between a system  
3 power line and the first power supply node.

1           29. The system of claim 25, wherein a source terminal  
2           of the second p-channel transistor of each memory cell is  
3           coupled to the first power supply node.

1           30. The system of claim 25, wherein a source terminal  
2           of the second n-channel transistor of each memory cell is  
3           coupled to the second power supply node, and a source  
4           terminal of the first n-channel transistor of each memory  
5           cell is coupled to a fourth power supply node, the fourth  
6           power supply node having the second reference voltage during  
7           the normal and data corruption modes of operation.

1           31. The system of claim 23, wherein the power control  
2           circuitry places the second reference voltage on the second  
3           power supply node during the normal mode of operation and  
4           causes a second voltage greater than the second reference  
5           voltage to appear on the second power supply node during the  
6           data corruption mode of operation.

1           32. The system of claim 31, wherein the second voltage  
2           is the first reference voltage.

1           33. The system of claim 31, wherein the power control  
2     circuitry comprises a first transistor coupled between the  
3     first power supply node and the second power supply node, the  
4     transistor being activated during a portion of the data  
5     corruption mode of operation and deactivated during the  
6     normal mode of operation.

1           34. The system of claim 33, wherein the power control  
2     circuitry comprises a second transistor coupled between the  
3     first power supply node and the second reference voltage, and  
4     a third transistor coupled between the second power supply  
5     node and the first reference voltage, the second and third  
6     transistors being activated during the data corruption mode  
7     of operation and deactivated during the normal mode of  
8     operation.

1           35. The system of claim 34, wherein during the data  
2     corruption mode of operation, the first transistor is  
3     activated prior to the second and third transistors being  
4     activated.

1           36. The system of claim 31, wherein the power control  
2   circuitry comprises a first transistor coupled between a  
3   first external voltage supply line and the first power supply  
4   node, and a second transistor coupled between a second  
5   external voltage supply line and the second power supply  
6   node, the first and second transistors being activated during  
7   the normal mode of operation and deactivated during at least  
8   a portion of the data corruption mode of operation.